CLAIMS

1. A clock recovery system comprising:

a first phase detector comparing a data signal to an output signal and generating control signals based on the comparison;

a first counter receiving the control signals and selecting a clock signal based on received control signals and adjusting the output signal to correspond to the selected clock signal;

a second phase detector comparing a reference clock signal to a delayed clock signal and generating control signals based on the comparison; and

a second counter receiving the control signals and the selected clock signal and selecting an offset clock signal based on the control signals and the selected clock signal.

2. The system of claim 1 further comprising a first multiplexer generating the output signal based on the selection from the first counter.

3. The system of claim 1 further comprising a second multiplexer generating the offset clock signal based on the selection from the second counter.

4. The system of claim 1 wherein the delayed clock signal is a clock signal that is at most one clock period out of phase of the reference clock signal.

5. The system of claim 1 wherein the delayed clock signal is dependent on the offset clock signal.

6. The system of claim 1 wherein the delayed clock signal is offset by the selected clock signal and a half a clock period of the offset clock signal.

7. A clock recovery method comprising:

generating a plurality of clock signals based on a reference clock signal;

selecting one of the plurality of clock signals based on a phase signal;

generating the phase signal based on the selected plurality of clock signals and a data signal;

generating a reference signal based on a reference clock signal and a delayed clock signal; and

adjusting the selected one of the plurality of clock signals based on the generated reference signal.

8. A digital clock recovery unit with harmonic lock prevention, comprising:

a phase generator receiving a clock signal and generating multiple phase-shifted versions of the clock signal;

a reference loop including a reference phase detector comparing two of the phase-shifted versions of the clock signal and driving a reference selector to cause selection of phase-shifted versions of the clock signal phase-shifted a predetermined amount, the reference loop forming a reference selection signal indicating a clock period of the clock signal;

a clock recovery loop including a phase detector comparing a phase-shifted version of the clock signal with a

data signal, the phase detector driving a selector to cause selection of a phase-shifted version of the clock signal having a constant phase with respect to the data signal;

the selector of the clock recovery loop limiting the selection of the phase-shifted version of the clock signal having a constant phase with respect to the data signal based on the reference selection signal.

9. A method of recovering a clock signal from a data stream comprising:

providing a reference clock signal approximate an expected frequency of the clock signal to a delay line;

determining a length of the delay line corresponding to a period of the reference clock signal;

iteratively selecting a recovered clock signal from the delay line based on a comparison of the recovered clock signal with a data signal, the recovered clock signal limited to a section of the delay line corresponding to the period of the reference clock signal.

10. The method of claim 9 wherein determining a length of the delay line corresponding to a period of the reference clock signal comprises comparing a first reference clock signal from a variable position on the delay line with a second reference clock signal from a fixed position on the delay line and adjusting the position of the variable position until the first reference clock signal and the second reference clock signal have a constant phase relationship.

11. The method of claim 10 wherein the constant phase

relationship is zero phase difference.

12. The method of claim 11 wherein the difference in position between the fixed position and the variable position indicates the length of the delay line corresponding to one clock period of the reference clock.

13. The method of claim 12 wherein the recovered clock signal is limited to positions along the delay line from the fixed position to the variable position.

14. The method of claim 13 wherein the recovered clock signal is selected from positions along the delay line that vary at a substantially constant rate, whereby the recovered clock signal is offset in frequency from the reference clock signal.

15. The method of claim 13 further comprising determining a sampling clock signal using the recovered clock signal and a fraction of the difference between the fixed position and the variable position.

16. The method of claim 15 wherein the fraction is one-half.

17. The method of claim 15 wherein the sampling clock signal and the recovered clock signal have a phase difference of approximately 90 degrees.

18. The method of claim 13 wherein the delay line

provides outputs at a fixed number of discrete points along the delay line, the difference between the fixed position and the variable position is N outputs, and the recovered clock signal is taken from output K, with the method further comprising selecting a sampling clock signal from the delay line from an output determined by adding a fixed fraction of N to K.

19. The method of claim 18 wherein the delay line provides outputs at a fixed number of discrete points along the delay line, the difference between the fixed position and the variable position is N outputs, and the recovered clock signal is taken from output K, with the method further comprising selecting a sampling clock signal from the delay line from an output determined by subtracting a fixed fraction of N to K.

20. A digital clock recovery unit comprising:

a digital phase locked loop comprising a phase detector, a low pass filter, and a delay element with a selectable output, the phase detector comparing a data signal with a selected output of the delay element to form a phase difference signal provided to the low pass filter, the low pass filter forming a selector signal to select the selected output, the selector signal being limited to a range indicated by a reference signal; and

a reference digital phase locked loop comprising a reference phase detector, a reference low pass filter, and the delay element with a reference selectable output, the reference phase detector comparing a fixed output of the delay

element with a reference selected output of the delay element to form a reference phase difference signal provided to the reference low pass filter, the reference low pass filter forming a reference selector signal to select the reference selected output, the reference selector signal forming the reference signal.

21. A clock recovery system comprising:

means for generating a plurality of clock signals differing in phase;

means for comparing a selected clock signal of the plurality of clock signals with a data signal to generate a change signal;

means for varying the selected clock signal based on the change signal and a range signal; and

means for comparing a fixed clock signal of the plurality of clock signals with a variable clock signal of the plurality of clock signals to generate a range signal.